

Appl No.: 10/533,188  
Amdt. dated 11/13/2007  
Reply to Office Action of July 13, 2007

#### REMARKS/ARGUMENTS

Claims 10, 28-35, and 38-39 remain pending after entry of the above amendments. Non-elected Claims 1-9, 11-27, and 36-37 have been canceled without prejudice.

Claims 10, 28-35, and 38-39 were rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,399,975 to Laing et al. ("Laing").

#### Response to Rejections

The Office Action asserted that Laing discloses all of the elements of each of Claims 10, 28-35, and 38-39. For the reasons noted below, it is respectfully submitted that such is not the case, and these claims are novel and patentable over Laing.

Laing's test method and apparatus are based on use of a *current-sensing* probe 5 that determines whether or not a pin connection is good based on the presence or absence of a *current* flowing through a current path in an IC device 9 in response to application of a voltage potential applied to the pin under test. As will become apparent, Laing's probe 5 is able to determine only whether or not current is flowing in the current path of the device 9. Laing fails to teach or suggest measuring voltage differences *within the device 9 itself* in response to applied voltage potentials, in the manner claimed in the present application.

Referring first to Figure 1, Laing describes a "bed of nails" in-circuit test (ICT) fixture 3 for testing the continuity of connections between the pins of an IC device 9 connected to a circuit board 7. Pins 11 and 13 are meant to be connected to the supply and ground rails, respectively, of the circuit board 7. These pins are connected to a signal pin 15 via respective diodes 17 and 19. The bed of nails applies a voltage of 5V to pins 11 and 13 and then switches the voltage that is applied to pin 15 between OV and 5V. Any current that is caused to flow within the IC device 9 is detected by an inductive current-sensing probe 5.

The structure of the probe 5 is set out in Figure 5. The tip of the probe includes a tuned circuit 47. The output of tuned circuit 47 is amplified by amplifier 49 and is then passed to an envelope detector 51.

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The operation of the test system is shown in Figure 6. Figure 6(i) shows the waveform of the voltage that is applied to pin 15 by the bed of nails. Figure 6(ii) shows the response of the tuned circuit 47 in the probe 5 in the case where the connections of pins 11, 13, and 15 to the circuit board 7 are good. Figure 6(iv) shows how the output of the envelope detector 51 within probe 5 builds up over successive cycles of the square wave signal that is applied to pin 15, in the case where the connections of pins 11, 13, and 15 are good. It is said at column 4, line 22 that the charge on capacitor 81 within the envelope detector 51 increases exponentially as further cycles of the Figure 6(i) waveform pass by. Figure 6(iv) shows the output voltage  $V_{out}$  from the envelope detector as a function of time.

The manner in which the current in the device 9 is detected by the current-sensing probe 5 is described at column 4, lines 13+. A predetermined test time is set, which starts with the beginning of the application of the train of voltage pulses to pin under test 15. When this predetermined time expires, the ATE system 1 samples the output voltage  $V_{out}$  from the envelope detector of the probe 5. If the sampled voltage is above a threshold voltage, pin connection 15 is good; otherwise it is not good.

It is important to clearly recognize that the voltage  $V_{out}$  is not a voltage present anywhere within the IC device 9 itself. Rather  $V_{out}$  is a voltage response of the envelope detector of the current-sensing probe 5.

This differs from the method described in Claim 10 of the present application in several respects.

Claim 10 specifies applying one or more first test signals to the first group of pins and measuring one or more respective first voltage differences occurring between the group of first pins and a reference voltage. Laing does not measure any voltage differences that might be associated with pins 11, 13, and 15 and resulting from the application of the Figure 6(i) waveform to pin 15. Although lines 26-31 of column 4 of Laing describe comparing the output voltage  $V_{out}$  to a threshold value, this is in fact the output voltage of the probe 5 and not the measurement of a voltage occurring in the IC device 9 that is being tested.

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Claim 10 also specifies that similar measurements are made on a second group of pins. Claim 10 then continues by specifying the step of "on the basis of the measurements, extracting and comparing a non-linear characteristic of the first and second groups of pins to obtain a measure of said continuity". While it is apparent that Laing will test different groups of pins, there is no disclosure in Laing of comparing measurements done on two different groups of pins in order to make deductions about the integrity of connections.

Claim 10 further requires the step of "comparing a non-linear characteristic of the first and second groups of pins". Nowhere in Laing is there any mention of examining a non-linear characteristic or behavior of the IC device 9 under test. Laing does mention exponential behavior in capacitor 81 (column 4, lines 21-23), but this is non-linear behavior of the circuitry within the probe § and not within the IC package 9 itself. Laing does not describe any step of comparing a non-linear characteristic of two different groups of pins in order to obtain a measure of continuity of connections of the pins to the circuit board.

For these reasons, Claim 10 is not anticipated by Laing.

Independent apparatus Claim 28 is not anticipated by Laing for reasons similar to those noted above. Claim 28 requires "a first tester for applying M test signals to the first group of pins and *measuring M voltage differences occurring between the first circuit node and a reference*", "a second tester for applying N test signals to a second group of pins expected to have a behaviour identical to or relatable to the first group of pins and *measuring N voltage differences occurring between a second circuit node connected to the second group of pins and a reference*", and "a processor responsive to the voltage differences for *deriving or comparing a non-linear characteristic* of the first and second groups of pins to obtain a measure of said continuity."

As previously noted, Laing does not measure any voltage differences that might be associated with pins 11, 13, and 15 and resulting from the application of voltage to pin 15. Thus, Laing lacks the claimed first tester and second tester. Additionally, as noted, Laing neither derives nor compares a non-linear characteristic of two groups of pins, and thus lacks the processor as claimed.

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For these reasons, Claim 28 is not anticipated by Laing.

Dependent Claims 29-35 and 38-39 likewise are not anticipated by Laing for at least the same reasons applicable to Claim 28. Additionally, Laing fails to teach or suggest the limitations in each of the dependent claims in combination with the limitations of Claim 28, and thus each dependent claim is patentable over Laing for this additional reason.

Conclusion

Based on the above amendments and remarks, it is respectfully submitted that all pending claims are patentable and the application is in condition for allowance.

It is not believed that extensions of time or fees for net addition of claims are required, beyond those, which may otherwise be provided for in documents accompanying this paper. However, in the event that additional extensions of time are necessary to allow consideration of this paper, such extensions are hereby petitioned under 37 CFR § 1.136(a), and any fee required therefor (including fees for net addition of claims) is hereby authorized to be charged to Deposit Account No. 16-0605.

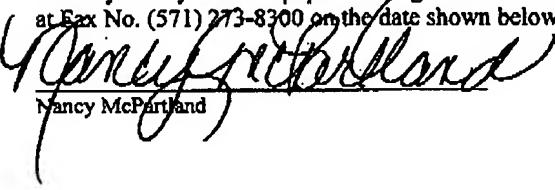
Respectfully submitted,

Donald M. Hill, Jr.  
Registration No. 40,646

CUSTOMER NO. 00826  
**ALSTON & BIRD LLP**  
Bank of America Plaza  
101 South Tryon Street, Suite 4000  
Charlotte, NC 28280-4000  
Tel Charlotte Office (704) 444-1000  
Fax Charlotte Office (704) 444-1111

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I hereby certify that this paper is being facsimile transmitted to the US Patent and Trademark Office at Fax No. (571) 273-8300 on the date shown below.

  
Nancy McParland

November 13, 2007  
Date